

100V N-Channel Power MOSFET

DESCRIPTION

The BLM08N10 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

KEY CHARACTERISTICS

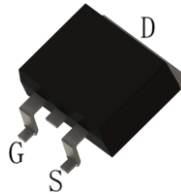
- $V_{DS} = 100V, I_D = 110A$
 $R_{DS(ON)} < 8m\Omega @ V_{GS}=10V$
- Special process technology for high ESD capability
- High density cell design for lower R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

100% UIS TESTED!

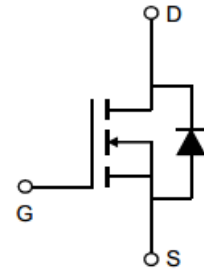
100% DVDS TESTED!



TO-220 Top View



TO-263 Top View



Schematic diagram

Package Marking And Ordering Information

Device Marking	Ordering Codes	Package	Product Code	Packing
M08N10	BLM08N10-P	TO-220	BLM08N10	Tube
M08N10	BLM08N10-B	TO-263	BLM08N10	Reel

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	110	A
Drain Current-Pulsed (Note 1)	I_{DM}	440	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D	211	W
Single pulse avalanche energy (Note 2)	E_{AS}	1100	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.71	$^\circ C/W$
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance ^(Note 3)	$R_{DS(ON)}$	$V_{GS}=10V, I_D=55A$	-	7.5	8	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=57A$	90	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$	-	6550	-	pF
Output Capacitance	C_{oss}		-	370	-	pF
Reverse Transfer Capacitance	C_{riss}		-	340	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=40A,$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	25	-	nS
Turn-on Rise Time	t_r		-	24	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	90	-	nS
Turn-Off Fall Time	t_f		-	40	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=30A$ $V_{GS}=10V$	-	162	-	nC
Gate-Source Charge	Q_{gs}		-	30	-	nC
Gate-Drain Charge	Q_{gd}		-	65	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. EAS condition : $T_j=25^\circ C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.

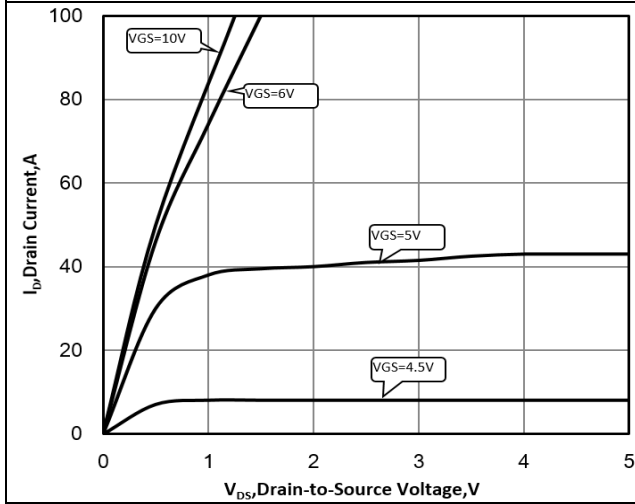
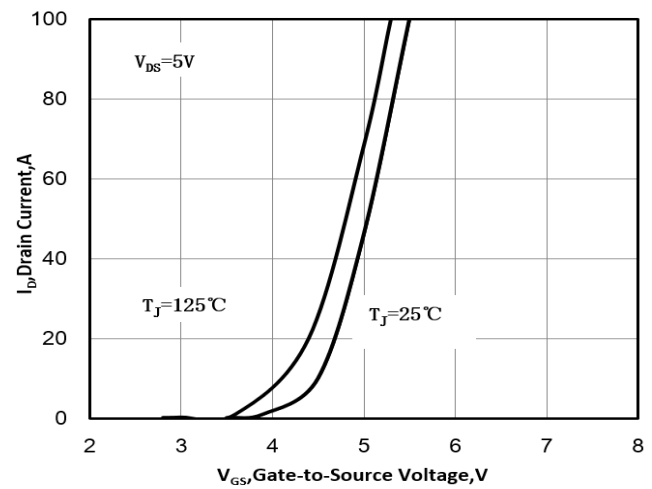
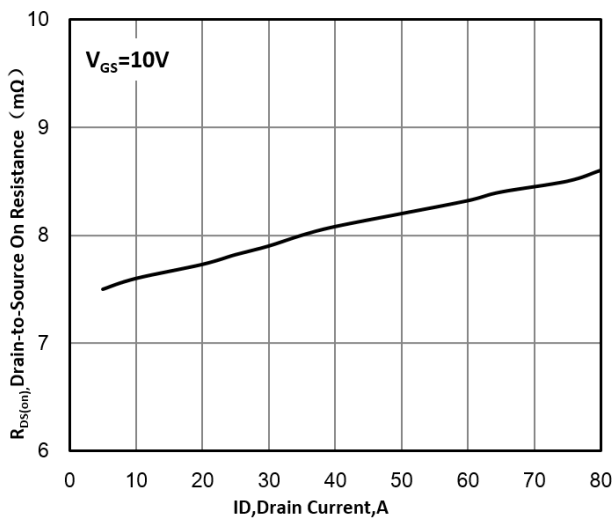
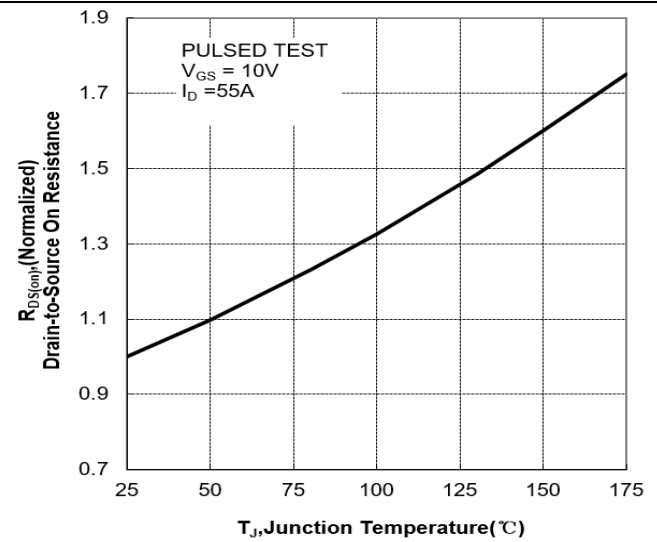
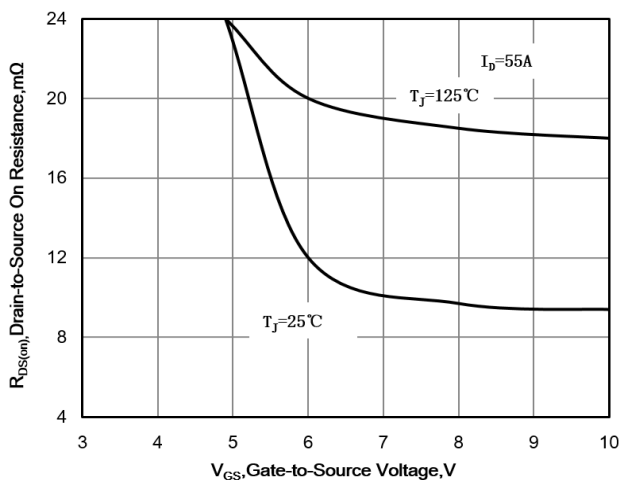
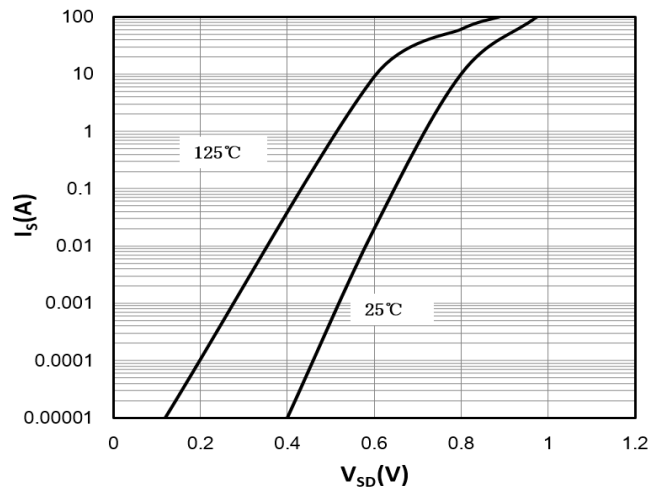
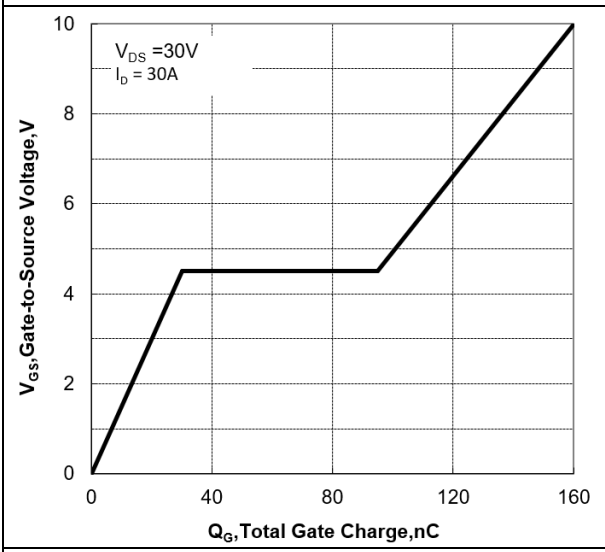
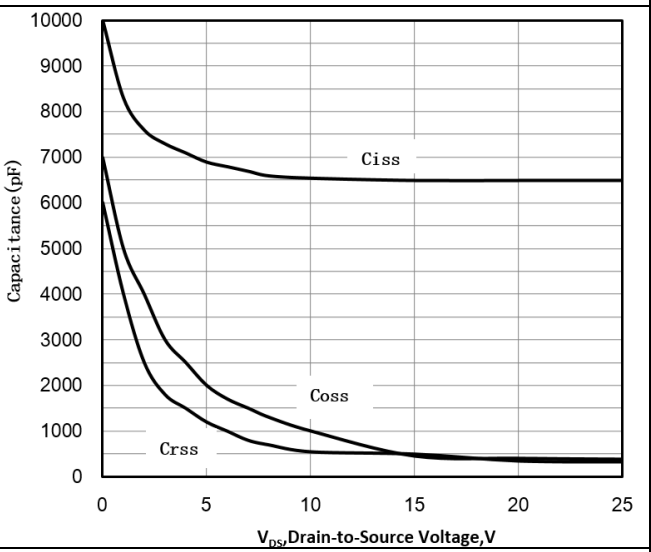
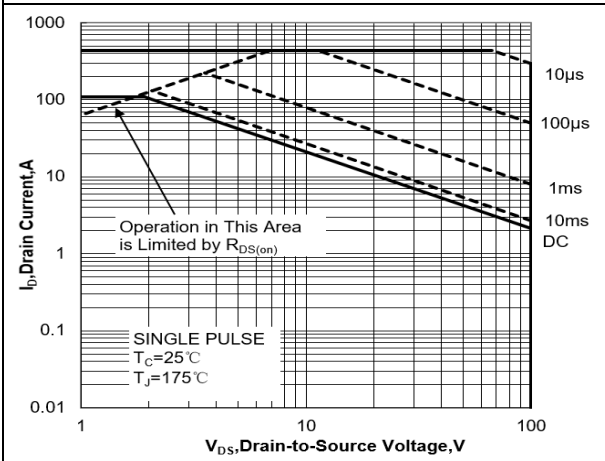
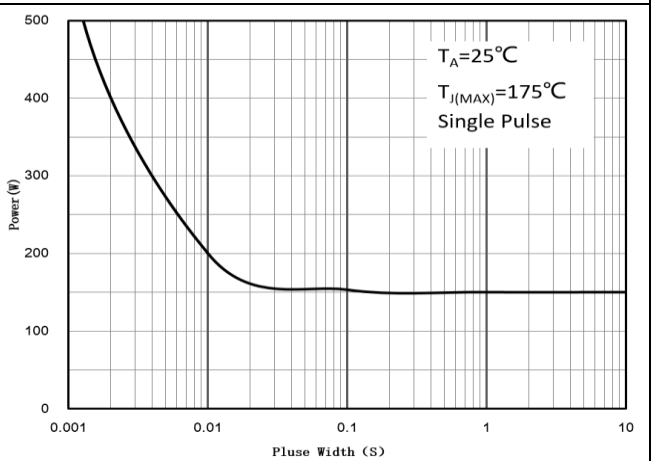
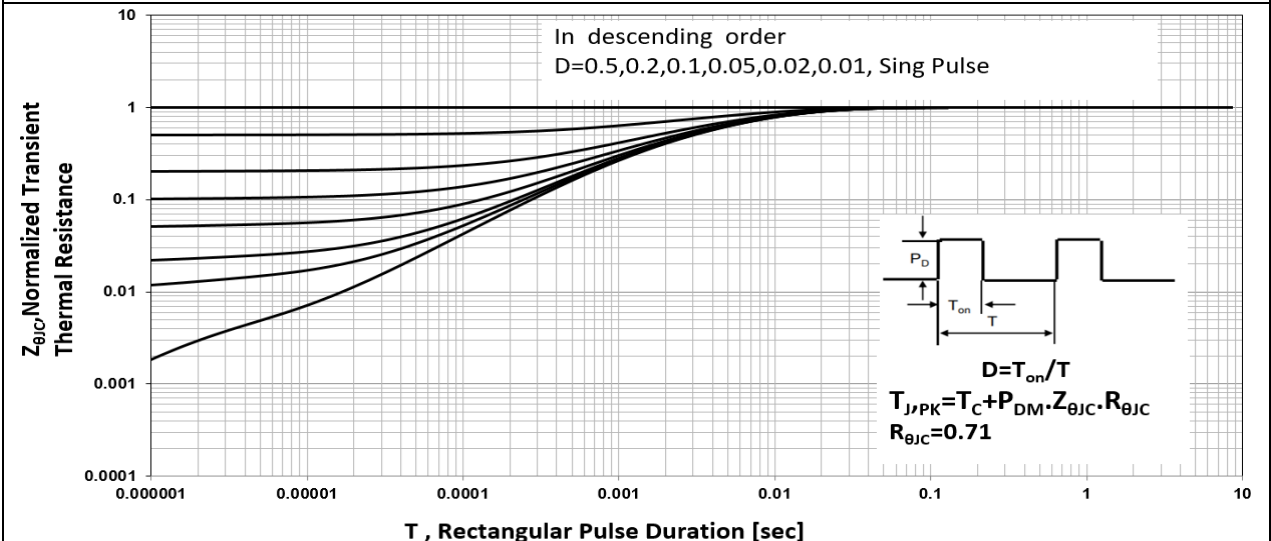
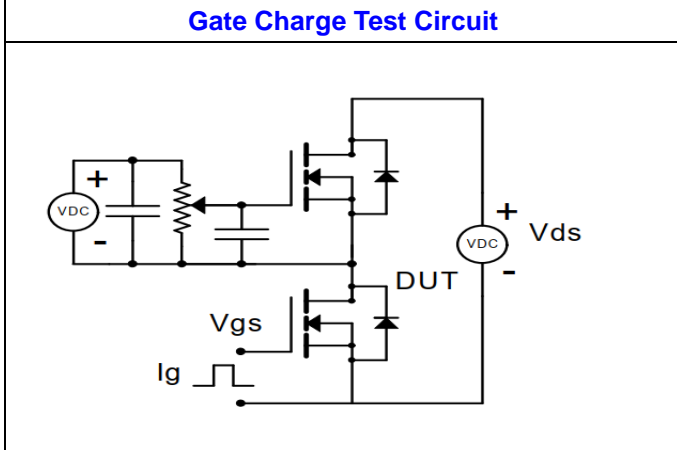
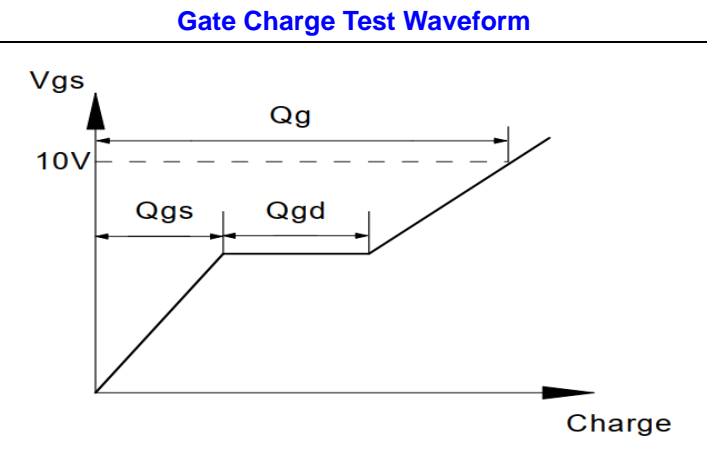
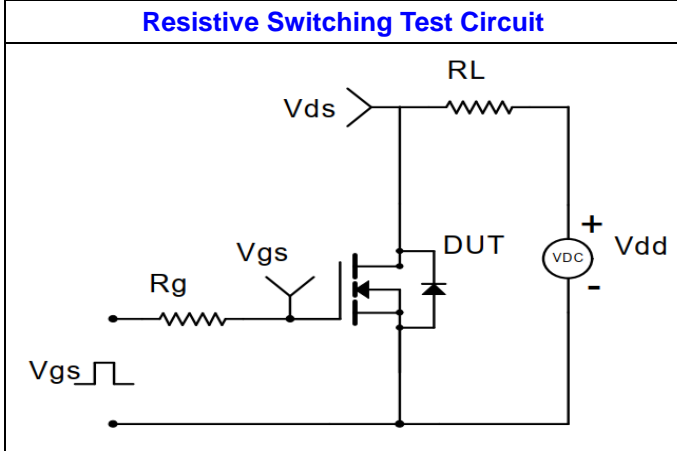
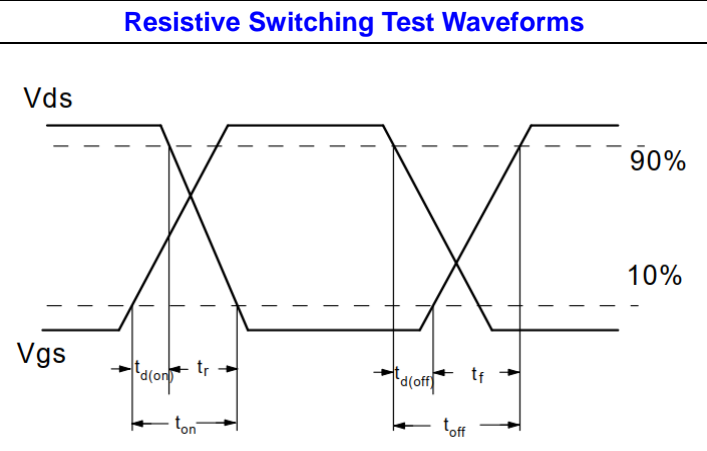
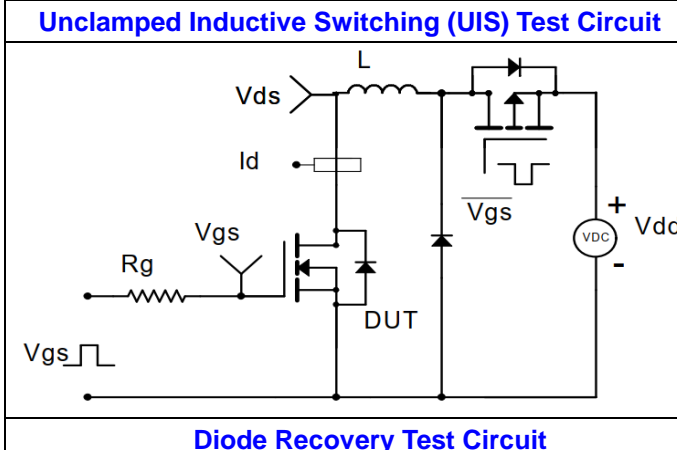
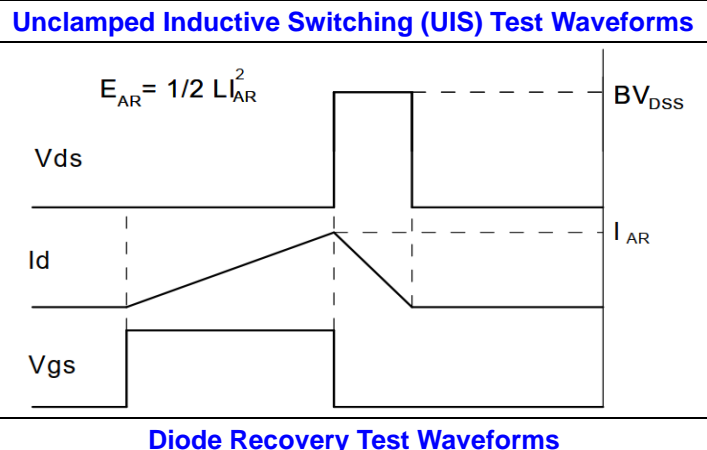
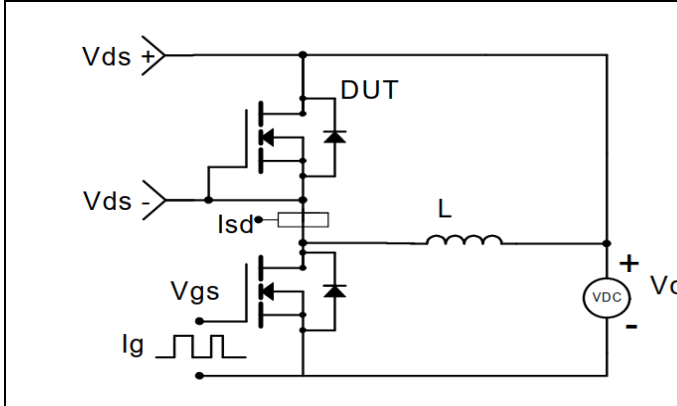
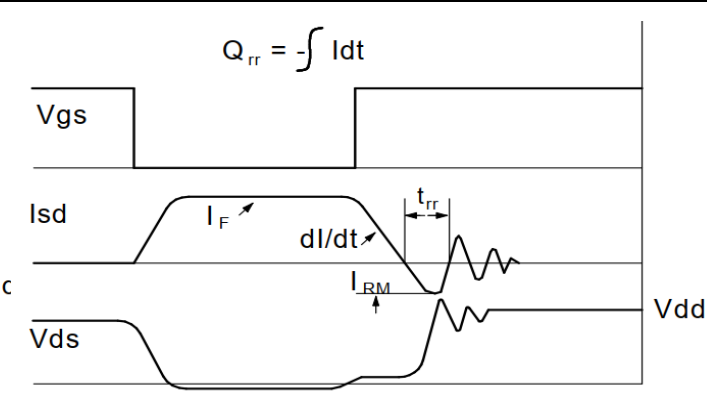
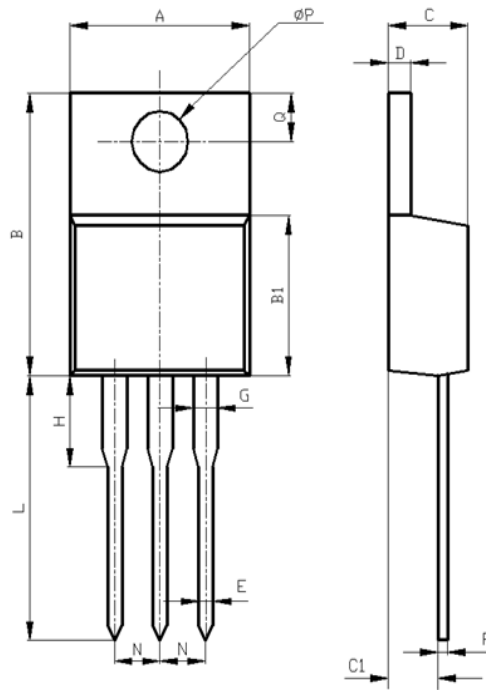
Characteristics Curves
Figure 1 Output Characteristics

Figure 2 Transfer Characteristics

Figure 3 On-Resistance vs. I_D and V_{GS}

Figure 4 On-Resistance vs. Junction Temperature

Figure 5 On-Resistance vs. V_{GS}

Figure 6 Body Diode Forward Voltage


Figure 7 Gate-Charge Characteristics

Figure 8 Capacitance Characteristics

Figure 9 Maximum Forward Biased Safe Operation Area

Figure 10 Single Pulse Power Rating Junction-to-Ambient

Figure 11 Normalized Maximum Transient Thermal Impedance


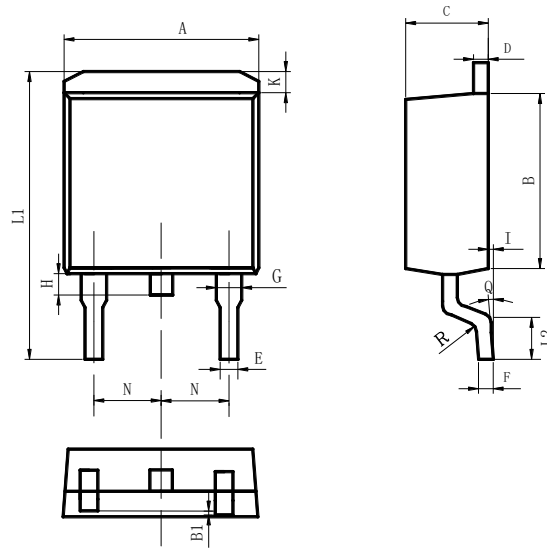
Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET (DUT) in a common-emitter configuration. A VDC source is connected to the drain through a resistor. The gate is driven by a pulse source Ig through a resistor Rg. A diode is connected in parallel with the MOSFET to provide a path for the gate current during the off-state.</p>	 <p>The graph plots Gate Voltage (Vgs) against Charge. The Vgs signal rises linearly to 10V, remains constant for a duration Qgs, and then falls linearly. The total area under the Vgs curve is labeled Qg. The falling edge is labeled Qgd.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET (DUT) in a common-emitter configuration. A load resistor RL is connected between the drain and a VDD source. The gate is driven by a pulse source Vgs through a resistor Rg.</p>	 <p>The graph shows the switching waveforms for Vds and Vgs. Vgs is a square wave. Vds shows a trapezoidal shape during the switching transitions. Key parameters are labeled: t_{d(on)} (delay to turn on), t_r (rise time), t_{d(off)} (delay to turn off), and t_f (fall time). The Vds levels are marked at 90% and 10%.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET (DUT) in a common-emitter configuration. A load inductor L is connected between the drain and a VDD source. The gate is driven by a pulse source Vgs through a resistor Rg. A diode is connected in parallel with the MOSFET.</p>	 <p>The graph shows the switching waveforms for Vds, Id, and Vgs. Vgs is a square wave. Id shows a linear ramp up during the turn-on transition. Vds shows a trapezoidal shape during the turn-on transition. The energy stored in the inductor is given by the equation: $E_{AR} = 1/2 L I_{AR}^2$. The Vds level is marked at BV_{DSS} and the Id level is marked at I_{AR}.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET (DUT) in a common-emitter configuration. A load inductor L is connected between the drain and a VDD source. The gate is driven by a pulse source Ig through a resistor Rg. A diode is connected in parallel with the MOSFET.</p>	 <p>The graph shows the switching waveforms for Vgs, Isd, and Vds. Vgs is a square wave. Isd shows a trapezoidal shape during the turn-on transition. Vds shows a trapezoidal shape during the turn-on transition. The reverse recovery time t_{rr} is indicated. The reverse current I_{RM} is also shown. The equation for reverse recovery charge is given as: $Q_{rr} = -\int Idt$.</p>

Package Description


Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ϕP	3.50	3.90

TO-220 Package



Items	Values(mm)	
	MIN	MAX
A	9.80	10.40
B	8.90	9.50
B1	0	0.10
C	4.40	4.80
D	1.16	1.37
E	0.70	0.95
F	0.30	0.60
G	1.07	1.47
H	1.30	1.80
K	0.95	1.37
L1	14.50	16.50
L2	1.60	2.30
I	0	0.2
Q	0°	8°
R	0.4	
N	2.39	2.69

TO-263 Package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shanghai Belling reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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